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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,750	09/25/2003	Chad A. Cobbley	MICS:0078--1 (FLE/MAN) (0	1056

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,750	COBBLEY ET AL.	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35,37-39,45,47-49,63 and 65-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35,37-39,45,47-49,63 and 65-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the amendment filed 10/17/05.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 35, 37-39, 45, 47-49, 63, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Huang (US006753206B2).

Pai teaches the device of claims 38-39, 48-49, and 66 as except for the stack being a shingle stack (defined in the instant specification where the die centers are not aligned) and for the at least two die being electrically functional.

Regarding claim 35, An integrated circuit comprising a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional.)**

Regarding the limitation where the at least two die are electrical functional, Pai teaches one of the die is a dummy die, but of the same material as the electrically functional die. Thus by forming a wire, the dummy die could then serve an electrical function. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Regarding claim 37. The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Regarding claim 38. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(It is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47)) Further, it is noted that the instant application teaches a "conventional stack" also.**

Regarding claim 39. The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Regarding claim 45. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate. **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)
wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional.)**

Regarding the limitation where the at least two die are electrical functional, Pai teaches one of the die is a dummy die, but of the same material as the electrically functional die. Thus by forming a wire, the dummy die could then serve an electrical function. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Regarding claim 48. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**,

each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate; **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47))**.

Regarding claim 47. The integrated circuit, as set forth in claim 45, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Regarding claim 49. The integrated circuit, as set forth in claim 45, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Regarding claim 63. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional.)**

Regarding the limitation where the at least two die are electrical functional, Pai teaches one of the die is a dummy die, but of the same material as the electrically functional die. Thus by forming a wire, the dummy die could then serve an electrical function. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Regarding claim 65. The integrated circuit package, as set forth in claim 63, wherein the topside surface area of one of the at least two semiconductor die is less

than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Regarding claim 67. The integrated circuit package, as set forth in claim 63, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Regarding claim 66. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47))**.

It would be obvious to one skilled in the requisite art at the time of the invention would modify Pai by including an electrically functional die and a shingle stack as taught by Huang to be an improvement with chips of varied sizes **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47))**.

3. Claims 68-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Hakey (US006627477B1).

Pai teaches the device of claims 68-70 as except for explicitly teaching that each die in the stack may successively thinner than the previous one.

Claim 68. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first

temperature; **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two die is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die**).

Claim 69. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate; **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.**

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two die is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die).**

Claim 70. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)
wherein each die in the stack is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die**).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Pai to include chips having a different thickness as suggested by Pai's description of the chips, Hakey teaching that the chips listed by Pai have different thicknesses.

Response to Arguments

4. Applicant's arguments with respect to claims 35, 37, 39, 45, 47, 49, 63, and 65, and 67 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 38, 48, and 66, the applicant argues that Huang does not teach a "shingle stack" as taught by the instant specification. However, as defined by the instant

specification, a 'shingle stack" is one where an upper stack overhangs a lower stack. Huang teaches this.

The applicant argues further, that in the lead frame of Huang, there is a mis-match of thermal expansions between the dies. Huang is used to show a die configuration and (with the amendment) that the dummy die of Pai could be used electrically. As Pai uses dies of the same material, thermal expansion differences is not an issue.

The applicant further argues that one could not modify Pai (in view of Huang) without changing the principle of Pai, in that Pai teaches a dummy die to prevent problems between dies. However, as Pai teaches the dummy die to be of the same material as the other die, it could easily be substituted for an electrically functional die (of the same material, thus avoiding the mis-matches) as suggested by the electrically functional die of Huang.

The applicant further argues that claim 38 is also allowable because claim 38 recites a first and second adhesive being curable at a first and second temperature and these are physical properties of the adhesives, and not process steps. However, the claims do not preclude the two curing temperature from being the same. Further, even though two adhesives may cure at different temperatures, that does not translate into different properties after curing or prior to curing, other than the temperature itself, a property that does not reflect any tangible difference in the product as claimed. It is noted that

this "property" is taught by Pai. even if the argument that this is a property and not a process were persuasive, the limitation is “anticipated by Pai.

The applicant argues that claims 68-70 are allowable as Hakey merely discloses a method of achieving coplanarity between chips and not "wherein each stack of at least two die is successively thinner than the previous die. However, Hakey was used to show that the die as described by Pai would have different thicknesses. with different thicknesses among two die, one must be successively thinner than the other die.

The applicant also argues that there is no motivation to combine Pai and Hakey. However, the examiner disagrees. Hakey was used to further describe something recited by Pai. Motivation was given within the rejection.

The applicant again argues that claim 38 is also allowable because claim 38 recites a first and second adhesive being curable at a first and second temperature and these are physical properties of the adhesives, and not process steps. However, the claims do not preclude the two curing temperature from being the same. Further, even though two adhesives may cure at different temperatures, that does not translate into different properties after curing or prior to curing, other than the temperature itself, a property that does not reflect any tangible difference in the product as claimed. It is noted that this "property" is taught by Pai. even if the argument that this is a property and not a process were persuasive, the limitation is “anticipated by Pai.

The argument regarding Moden was persuasive and Moden has been removed from the rejection, no new reference being added.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

February 13, 2006